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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number 09/891,523

Filing Date June 27, 2001

OCT 12 2001

First Named Inventor RAKVIC et al

Group Art Unit 2185

Technology Center 2100

Examiner Name Not assigned

Attorney Docket Number 2207/1123601

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
MI		Agarwal et al, "Column-Associative Caches: A Technique for Reducing the Miss Rate of Direct-Mapped Caches", Proceedings, The 20 th Annual Intl Symposium on Computer Architecture, IEEE Computer Society, Technical Committee on Computer Architecture, Association for Computing Machinery SIGARCH, pp 169-190, San Diego, California, May 16-19, 1993	
MI		Alexander et al, "Distributed Prefetch-buffer/Cache Design for High Performance Memory Systems", Proceedings, Second Intl Symposium on High-Performance Computer Architecture, IEEE Computer Society, Technical Committee on Computer Architecture, pp 254-263, San Jose, California, February 3-7, 1996	
MI		Burger et al, "The SimpleScalar Tool Set, Version 2.0", <i>Computer Sciences Department Technical Report</i> , No. 1342, The University of Wisconsin, Madison, Wisconsin, June 1997	
MI		Edmondson et al, "Internal Organization of the Alpha 21164, a 300-MHz 64-bit Quad-issue CMOS RISC Microprocessor", <i>Digital Technical Journal</i> , Vol. 7, No. 1, pp 119-135, 1995	
MI		Hill, Mark D., "A Case for Direct-Mapped Caches", <i>Computer</i> , pp 25-40, December 1988	
MI		Juan et al, "The Difference-bit Cache", Proceedings, The 23 rd Annual Intl Symposium on Computer Architecture, ACM SIGARCH, IEEE Computer Society, TCCA, pp 114-120, Philadelphia, Pennsylvania, May 22-24, 1996	
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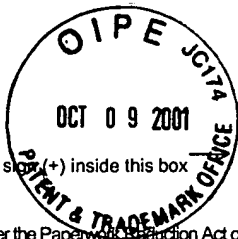
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Examiner Name	Not assigned
Attorney Docket Number	2207/1123601

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MI		Rau et al, "Pseudo-Randomly Interleaved Memory", Proceedings, The 18 th Annual Intl Symposium on Computer Architecture, Association for Computing Machinery, pp 74-83, Toronto, Canada, May 27-30, 1991	
MI		Rivers et al, "On Effective Data Supply for Multi-Issue Processors", Proceedings, Intl Conference on Computer Design, VLSI in Computers and Processors, IEEE Computer Society Technical Committee on Design Automation, IEEE Circuits and Systems Society, pp 519-528, Austin, Texas, Oct. 12-15, 1997	
MI		Sánchez et al, "A Locality Sensitive Multi-Module Cache with Explicit Management", Proceedings of the 1999 Intl Conference on Supercomputing, ICS '99, Rhodes, Greece	
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MI		Wilson et al, "Designing High Bandwidth On-Chip Caches", "The 24 th Annual Intl Symposium on Computer Architecture, Conference Proceedings, ACM, pp 121-132, Denver, Colorado, June 2-4, 1997	
MI		Wilton et al, "An Enhanced Access and Cycle Time Model for On-Chip Caches", Digital WRL Research Report 93/5, Palo Alto, California, July 1994	

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